REMARKS

Status of the Claims

Applicants request the Examiner to reconsider the application as amended. Claims 1-39 are pending. Claims 23-39 have been withdrawn from consideration. Claims 1 and 18 have been amended.

Claim 1 has been amended to recite "a recessed region extending to an underlying gate dielectric." Support for this amendment can be found, for example, in Applicants' specification page 5-8 (paragraphs [0021] to [0029]), page 10 (paragraph [0036]), and in FIGS. 1-5.

Claim 18 has been amended to recite "at least two recessed regions extending to an underlying gate dielectric." Claim 18 has been further amended to recite "said recessed regions defining the position and dimensions desired for at least one n-FET gate and at least one p-FET gate" and to recite an alloy layer with a p-FET work function." Claim 19 has been amended to recite "electroplating a filler gate metal on said seed layer and said alloy layer to fill and overfill said recessed regions." Support for these amendments can be found, for example, in Applicants' specification page 7 (paragraph [0028]) and in FIG. 3.

Rejection of Claims 1, 2, 4, 9, and 10 Under 35 U.S.C. § 102(b) in view of Lopatin

Claims 1, 2, 4, 9, and 10 were rejected under 35 U.S.C. § 102(b) as allegedly being anticipated by U.S. Patent No. 6,440,830 to Lopatin ("Lopatin"). According to the Examiner, "Lopatin teaches a method for making a metal gate for a field effect transistor, said metal gate comprising plated material, said method comprising . . . selecting a

substrate 100 having a top surface and a recessed region 202 extending below said top surface . . . ." (Office Action, page 2).

While not acquiescing to the Examiner's rejection, Applicants have amended claim 1 to recite "a recessed region extending to an underlying gate dielectric." In contrast to Applicants' amended claim 1, Lopatin does not teach that its recessed region extends to an underlying gate dielectric. Instead, Lopatin teaches that "a polysilicon gate **104** [is] formed on a surface **106** of the semiconductor substrate **102**." (Lopatin, col. 2, ll. 16-18; *see also* Lopatin FIG. 1). Loptain further teaches that its disclosed trench does not extend to an underlying gate dielectric but, instead, extends to this conductive polysilicon gate material (*see e.g.*, Lopatin, FIG. 2). Therefore, for at least this reason, Lopatin fails to teach or suggest amended claim 1.

Rejection of Claim 3 Under 35 U.S.C. § 103(a) over Lopatin in view of Seibel

Claim 3 has been rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over Lopatin in view of U.S. Patent No. 6,777,317 to Seibel ("Seibel"). Applicants submit that this rejection is obviated in view of amended claim 1. In particular, Applicants not that nothing in Seibel overcomes the deficiencies of Lopatin in teaching or suggesting that a filler gate metal can be electroplated into a recessed region that extends to an underlying gate dielectric. Accordingly, for at least this reason, applicants submit that claim 3 is in immediate condition for allowance.

Rejection of Claim 6 Under 35 U.S.C. § 103(a) over Lopatin in view of Andricacos

Claim 6 has been rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over Lopatin in view of U.S. Patent No. 6,188,120 to Andricacos et al. ("Andricacos"). Applicants submit that this rejection is obviated in view of amended claim 1. In particular, Applicants not that nothing in Andricacos overcomes the deficiencies of Lopatin in teaching or suggesting that a filler gate metal can be electroplated into a recessed region that extends to an underlying gate dielectric. Accordingly, for at least this reason, applicants submit that claim 6 is in immediate condition for allowance.

Rejection of Claim 5 Under 35 U.S.C. § 103(a) over Lopatin in view of Siebel and Horji

Claim 5 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Lopatin in view of Siebel and U.S. Patent No. 6,255,187 to Horji ("Horji"). Applicants submit that this rejection is obviated in view of amended claim 1. In particular, Applicants not that the teachings of the combined references fail to overcome the deficiencies of Lopatin in teaching or suggesting that a filler gate metal can be electroplated into a recessed region that extends to an underlying gate dielectric. In this regard, Applicants note that Horji, as with Lopatin, teaches the use of conductive polysilicon between its disclosed substrate and trench (*see, e.g.*, Horji, col. 5, ll. 16-17 "[r]eferring to FIG. 1A, a plurality of pads 12 are formed of doped polysilicon over a

semiconductor substrate 10."). Accordingly, for at least this reason, applicants submit that claim 5 is in immediate condition for allowance.

Rejection of Claims 7, 8, and 11-17 Under 35 U.S.C. § 103(a) over Lopatin in view of Horji

Claims 7, 8, and 11-17 have been rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over Lopatin in view of Horji. For at least the reasons discussed above, Applicants submit that this rejection is obviated in view of amended claim 1. Accordingly, applicants submit that claims 7, 8, and 11-17 are in immediate condition for allowance.

Rejection of Claims 18 and 19 Under 35 U.S.C. § 103(a) over Gao in view of Doczy and Lopatin

Claims 18 and 19 have been rejected under 35 U.S.C. § 103(a) over U.S. Patent No. 6,873,048 to Gao et al. ("Gao") in view of U.S. Published Application No. 2005/0037557 to Doczy ("Doczy") and Lopatin. The Examiner acknowledged that Gao "fails to teach 1) selectively plating a layer allowing for a p-FET work function on the at least one p-FET gate and 2) annealing the metal layers deposited over the at least one p-FET gate to form an annealed layer with a p-FET work function." (Office Action, page 8). Nevertheless, the Examiner maintained that "it would have been obvious to one with ordinary skill in the art at the time of the invention to modify Gao and deposit the p-FET work function metal by electroplating for the benefit of applying a selective deposition technique." (Id.). The Examiner further maintained that "it would have been obvious to one with ordinary skill in the art at the time of the invention to modify Gao in view of

Doczy and perform an annealing step after the electrodeposition of the metal . . . ." (*Id.* at 9).

While not acquiescing to the Examiner's rejection, Applicants have amended claim 18 to recite "at least two recessed regions extending to an underlying gate dielectric." Applicants have further amended claim 18 to recite "said recessed regions defining the position and dimensions desired for at least one n-FET gate and at least one p-FET gate" and "annealing the metal layers deposited over the at least one p-FET gate to form an alloy layer with a p-FET work function." Applicants submit that the combination of cited references fail to teach or suggest all of the recitation of claim 18, as amended. In particular, Applicants submit that the combination of references fail to teach or suggest a method of making a gate having a recessed region for at p-FET gate that extends to an underlying gate dielectric and includes an annealed alloy with a p-FET work function. Applicants note, in this regard, that the portion of Loptain relied on by the Examiner fails to teach or suggest an annealing step in such a context. Instead, Loptain teaches that annealing should occur "to form reliable electrical contact between the high conductivity metal **306**, the barrier material **302**, and the polysilicon gate **104**." (Lopatin, col. 4, ll. 42-44). Such disclosure fails to provide the requisite motivation and reasonable expectation of success necessary for modification of the other cited references in order to meet all of the recitation of amended claim 18.

Rejection of Claim 20 Under 35 U.S.C. § 103(a) over Gao in view of Doczy, Lopatin, and Seibel

Claims 7, 8, and 11-17 have been rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over Gao in view of Doczy, Lopatin, and Seibel. For at least the reasons discussed above, Applicants submit that this rejection is obviated in view of amended claim 18. Accordingly, applicants submit that claim 20 is in immediate condition for allowance.

Rejection of Claims 21 and 22 Under 35 U.S.C. § 103(a) over Gao in view of Doczy, Lopatin, and Forbes

Claims 21 and 22 have been rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over Gao in view of Doczy, Lopatin, and U.S. Published Application No. 2004/0036129 to Forbes et al. ("Forbes"). For at least the reasons discussed above, Applicants submit that this rejection is obviated in view of amended claim 18. Accordingly, applicants submit that claims 21 and 22 are in immediate condition for allowance.

Conclusion

In view of the foregoing, the rejections should be withdrawn and all pending claims should be allowed.

If prosecution may be further advanced, Examiner is invited to telephone the undersigned to discuss this application.

Applicants believe no fees are due in conjunction with the filing of this Amendment. However, if any additional fees are due, such as a fee for a further extension of time, please charge the fees to Deposit Account No. 50-0510.

Dated: 7-13-05

Respectfully submitted,

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